16.384 MHz Clock Generation for SMX/PAC

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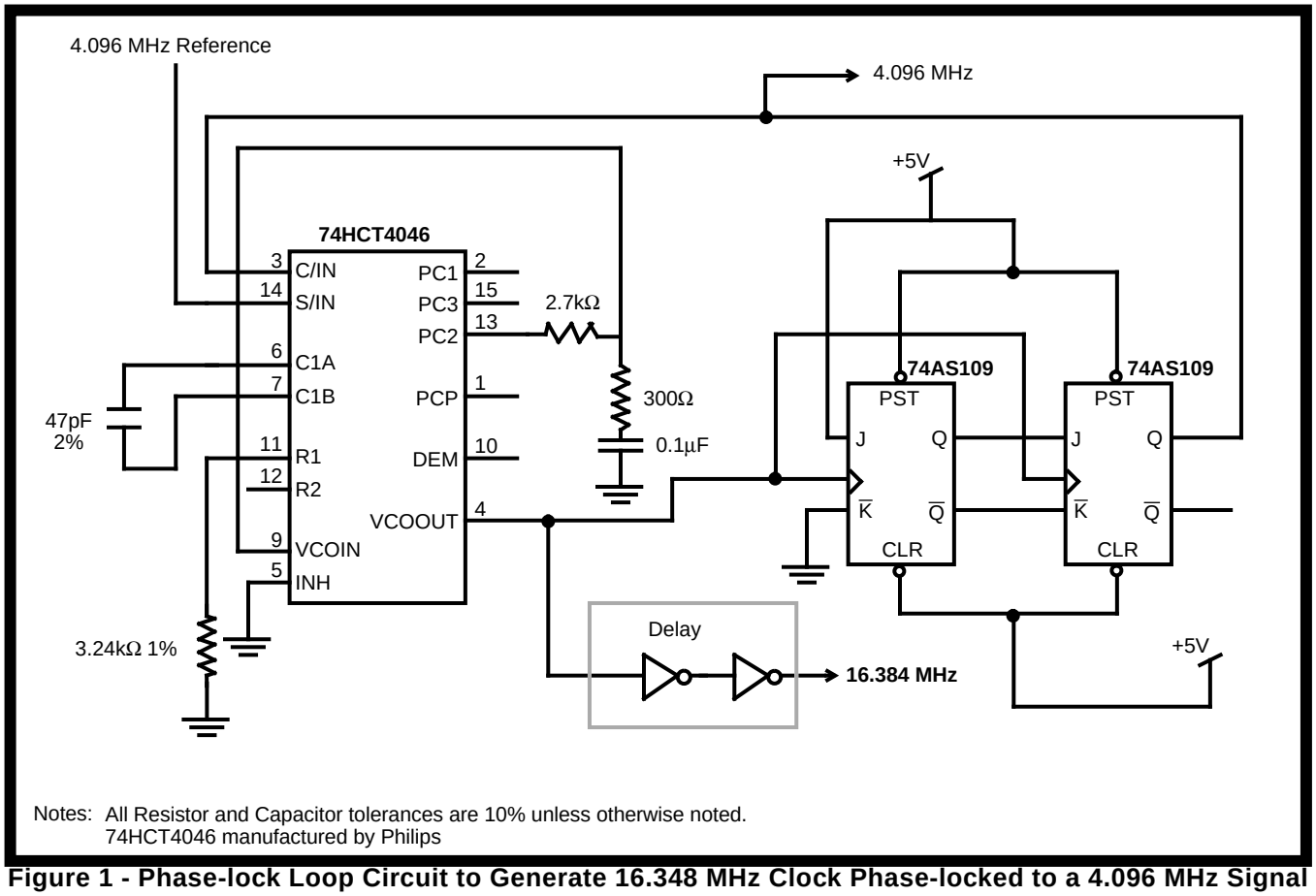
In typical applications using the MT9080 (SMX) and MT9085 (PAC), it is necessary to provide a 16.384 MHz signal phase-locked to the system 4.096 MHz clock. If the 4.096 MHz clock is derived from a 16.384 MHz source, the two signals can be used directly. In systems where only a 4.096 MHz signal is available, the 16.384 MHz clock can be generated using a phase-locked loop (PLL). An example of a PLL circuit is illustrated in Figure 1 below.

In the circuit of Figure 1, the divide-by-four counter inserts a delay (*t* nsec) in the PLL feedback loop, which results in VCO_{OUT} leading $COMP_{IN}$ by approximately *t* nsec. The setup time requirements of the MT9085 state that the falling edge of the 4.096 MHz clock can lag the rising edge of the 16.384 MHz clockby a maximum of 10 nsec, and the falling edge of the 4.096 MHz clock can lead the rising edge of the 16.384 MHz clock by a maximum of 25 nsec. Therefore, a very low propagation delay (less than 10 nsec) divide-by-four counter must be selected. If *t* is greater than 10 nsec, the 16.384 MHz signal must be delayed to meet the MT9085 setup time requirements.

Figure 1 shows a synchronous divide-by-four counter that has a delay in the range of 3.5 to 9.0 nsec (0 to 70 °C) using AS devices. Theoretically, this will meet the timing requirements (10 nsec), however, if a larger safety margin is required a delay element (inverter/buffer chain or programmable delay element) can be used to adjust the 16.384 MHz clock signal.



Notes: All Resistor and Capacitor tolerances are 10% unless otherwise noted.
74HCT4046 manufactured by Philips

Figure 1 - Phase-lock Loop Circuit to Generate 16.348 MHz Clock Phase-locked to a 4.096 MHz Signal

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